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Date : April 6, 2005 **Pages (including cover) :** 6

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Re: Our Docket No. 57265 (45107)
U.S. Serial No. 10/089,907

To :	**Fax**	**Phone**
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Docket No. 57265 (45107)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	X. Nie		
U.S. SERIAL NO.:	10/089,907	GROUP:	2183
FILED:	July 9, 2002	EXAMINER:	D. Pan
FOR:	PROCESSOR SYSTEM, ESPECIALLY A PROCESSOR SYSTEM FOR COMMUNICATIONS DEVICES		

CERTIFICATE OF FACSIMILE TRANSMISSION

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By: _____
Steven M. Jensen

Commissioner for Patents
P.O. Box 1450
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Sir:

RESPONSE TO OFFICE ACTION

Applicant is in receipt of the Office Action dated January 6, 2005 of the above-referenced application. Applicant responds to the Office Action as follows.

Applicant appreciates the notification of allowable subject matter, i.e., that claim 19 is merely objected to and would be allowable if rewritten in independent form.

Applicant's claimed invention is directed to a processor system with a processor unit for executing instructions, the processor unit including an instruction executing means made up of a plurality of executing units operable in parallel for parallel execution of instructions, at least a first executing unit connected to a first data bus, and a second executing unit connected to a second data bus with a higher transmission rate than the first data bus.

For example, as shown in FIG. 1, processor unit 1 can include two executing units 5, 7 for executing instructions in parallel. At least one of the executing units (e.g., executing unit 7) is structured as simply as possible to reduce complexity of design, so that only a limited number of functions or instructions can be executed, while at least one other executing unit (e.g., executing unit 5) can execute all possible functions or instructions (see specification at page 6, line 25 to page 7, line 5).

As shown in FIG. 2, the processor unit 1 is connected inside the processor system to two different data buses 9 and 10, where the data bus 9 has a higher transmission rate than the data bus 10 (see specification at page 9, lines 13-15). The processor unit 1 can access only the data bus 9 with its executing unit 7, whereas the executing unit 5 can use both data buses 9 and 10 (see page 9, lines 15-18).

Because the second executing unit 7 preferably only serves to execute a data block movement instruction, it is advantageously connected to the data bus 9 with a relatively high transmission rate, as compared to protocol processing performed by the first executing unit 5 over the data bus 10. According to this arrangement, the executing unit 7 is simplified such that it handles only data transfers which are executed at maximum speed.

Claims 13-16 and 20-24 were rejected under 35 USC §103(a) as being unpatentable over U.S. Patent 5,559,986 to Alpert et al. (hereinafter "Alpert") in view of U.S. Patent 5,841,771 to Irwin et al. (hereinafter "Irwin"). Claims 17 and 18 were rejected under 35 USC §103(a) as being unpatentable over Alpert in view of Irwin, and further in view of U.S. Patent 4,196,470 to Berg. These rejections are respectfully traversed.

Alpert does not teach or suggest a processor system including at least two data buses connected to two executing units, respectively, one of the data buses having a lower transmission rate than another of the data buses.

Referring to column 5, lines 24-51 and FIG. 2 of Alpert, microprocessor 200 includes a prefetcher 201 for prefetching instructions from main memory and a decoder 202 for decoding the prefetched instructions, the decoder 202 being coupled with two execution pipeline units 203 and 204 (referred to as the "u-pipe" and the "v-pipe" respectively).

However, Alpert does not teach or suggest first and second executing units connected to first and second data buses, respectively, or where the transmission rate of a first data bus is lower than the transmission rate of a second data bus.

The Irwin reference fails to remedy the above-noted deficiencies of Alpert. Irwin does not teach or suggest a plurality of executing units operable in parallel, or two data buses having different transmission rates.

For example, FIG. 9 of Irwin depicts the interface of a switching apparatus between several data buses and communication links. The interface includes an access unit 500 (shown in FIG. 7), which is split into two functional access units 501 and 502, the access unit 501 serving a lower group of ports 1-4 and the access unit 502 serving an upper group of ports 5-8, each port corresponding to a respective communication link (see column 18, line 63 to column 19, line 3).

FIG. 10 of Irwin is a block diagram of circuitry used in one of the access units, e.g., the access unit 501. The access unit 501 includes a group of eight latches 601-608, the latches being paired to receive data octets from one of the ports via an 8-lead bus (see column 21, lines 5-15). Each of the even numbered latches 602, 604, 606, and 608 is clocked by a clock signal to register an octet, and each of the latches 601, 603, 605, and 607 is clocked by another clock signal, both clock signals being inversely phased with respect to each other (see column 21, lines 18-27). The four words registered in each of the four pairs of latches 601-608 are continuously driven onto respective groups of 16 leads in a local ports bus 644, and multiplexers 727 and 728 are separately controlled to select header words and payload words, respectively, from the local ports bus 644 (see column 21, lines 27-34).

Referring to column 24, line 59 to column 25, line 13 of Irwin, as cited in the Office Action, each cell as read from one of the ports includes **four header octets H01-H04** and a fifth header error check octet HEC, which is twice as long as the header octets H01-H04; also, the cells include **payload octets P01-P48**. In Irwin, the header octets are latched in parallel onto the receive header bus 544, while the payload octets are transmitted in groups of four octets over the receive TDM bus A 546 having a maximum operating bit transfer rate of about 1.2 Gb/s (see column 25, lines 7-12).

Irwin does not teach or suggest a plurality of executing units that can be operated in parallel. Irwin merely discloses a plurality of **latches**, which are not equivalent to executing units for executing instructions in parallel, as recited in the Applicant's claimed invention.

Irwin also does not teach or suggest a plurality of buses connected to a plurality of executing units. Instead, Irwin discloses data buses for header octets (i.e., the receive header bus 544) or for payload octets (i.e., the receive TDM bus A 546).

Also, there is no teaching or suggestion of two data buses having different transmission rates. In Irwin, the TDM bus A 546 has a maximum operating bit transfer rate of about 1.2 Gb/s, but the transfer rate of the receive header bus 544 is not specified.

Since Irwin does not teach or suggest data buses corresponding to a plurality of executing units (but instead discloses **latches**, and data buses for header octets) or two data buses having different transmission rates, it cannot be combined with the microprocessor taught by Alpert to somehow produce the Applicant's claimed invention.

For at least the reasons discussed above, the proposed combination of Alpert in view of Irwin does not teach or suggest the Applicant's claimed invention. Therefore, independent claim 13 and claims depending therefrom are patentable over the proposed combination.

It is believed that the claims are now in condition for allowance. However, if there are any outstanding issues, the Examiner is urged to call the Applicant's representative at the telephone number listed below.

Respectfully submitted,

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Date: April 6, 2005

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